

ABSTRACT

A method for forming a non-volatile memory cell includes depositing an oxide layer over a component stack including a dielectric layer over a first conductive layer. A portion of an upper section of the oxide layer is removed such that the dielectric layer is exposed. The dielectric layer and a remainder of the oxide layer upper section are removed such that upper surfaces of the oxide layer and the first conductive layer are substantially planar. A second conductive layer is formed over the upper surfaces of the first conductive layer and the oxide layer. A non-volatile memory array is formed including multiple spaced and parallel bit lines in a substrate surface. Multiple stacked layers, including an electron trapping layer, are on the substrate surface over the bit lines. Multiple spaced word lines are over the stacked layers. The word lines are parallel to one another and perpendicular to the bit lines.